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Method of Its Fabrication

English Translation of International Application Including

Applicant's Preliminary Amendment

Showing the Changes

Field Effect Transistor and Method of Its Fabrication

~~Specification~~ BACKGROUND OF THE INVENTION.

1. Field of the Invention.

The invention relates to a field effect transistor provided with a vertically oriented semiconductor column of a diameter in the nanometer range (nano-wire) disposed between a source electrode and a drain electrode and annularly surrounded at an insulating space by a gate electrode as well as to a method of its fabrication.

2. The Prior Art.

Thin layer transistors are known in which semiconductor material is deposited in a planar arrangement on flexible substrates. However, mechanical stresses on the substrates easily lead to a release of the semiconductors from the substrate or to other damages and, hence, to functional failure.

It has already been proposed to fabricate transistors of the nanometer range by the formation of ion trace channels by ion bombardment in a foil composite consisting of two plastic foils and an intermediate layer of metal and by sensitizing the ion trace channels for subsequent etching. Semiconductor material is injected into the etched micro-holes by electro deposition or chemical bath precipitation. Source electrodes and drain electrodes are formed by subsequently metalizing the upper and lower surface of the foil compound. The center layer of metal serves as the gate electrode.

The advantage of the cylindrical and vertical arrangement of these transistors is the mechanical robustness since the foil is flexible and extensible. Moreover, the organic foil material is substantially softer than the inorganic semiconductor material. As a result, occurring bending, shear and compressive forces are almost completely absorbed by the foil material so that under bending, flexing and tensile forces the characteristic curve of the transistor and other electrical parameters remain substantially constant.

Since micro-holes can be fabricated down to 30 nm and filled with semiconductor material, transistors on the nanometer scale can be fabricated without lithography and without any masking technique.

Depending upon the type of precipitation of the semiconductor material, the process leads to polycrystalline semiconductor columns. The ration of length to diameter of the semiconductor columns is also limited by the required crystal growth within the micro-holes. Overall, the method of fabricating the transistors is still too complex since hitherto the ion bombardment can be carried out only in select scientific environments.

OBJECT OF THE INVENTION.

It is an object of the invention to provide a field effect transistor of the type initially referred to which can be fabricated with monocrystalline semiconductor columns even without ion irradiation. A suitable simple and industrially applicable method of its fabrication is to be provided in connection therewith.

SUMMARY OF THE INVENTION.

In accordance with the invention, the object is accomplished by the characteristics of claims 1 and 2. Useful embodiments are the subject of the sub-claims.

In accordance therewith, the semiconductor columns are embedded in a first and in a second insulating layer between which there is provided a metal layer extending outwardly as a gate electrode. The ends of the metal layer which upwardly extend through the insulating layer are partially converted to an insulator or partially removed and replaced by an insulating material.

Such a transistor can be fabricated by the following method steps:

- free-standing semiconductor columns are grown vertically on a conductive substrate;
- a first insulating layer is deposited on the semiconductor columns;
- onto which a first conductive metal layer and a second insulating layer are deposited thereafter;
- the resulting laminate is etched planar to the point of removing the portion of the first metal layer covering the semiconductor columns;
- the ends of the metal layer penetrating to the surface of the laminate are etched back in accordance with their metal and a third insulating layer is deposited on the laminate whereupon the laminate is again etched planar;
  or
  the ends of the metal layer penetrating to the surface are converted to an insulator by oxidation or nitriding;
- finally depositing a second metal layer on the laminate.

Compared to current vertical nano-transistors, the transistor offers the following advantages:

- The structure of the field effect transistor allows for an extremely high packing density and extremely small dimensions without any need to apply lithographic processes.
- The substrates used may be rigid or flexible.

- Ion beams are not necessarily required for the fabrication.
- The process makes possible the growth of mono-crystalline semiconductor columns. Transistors with mono-crystalline semiconductors have higher switching rates than those with poly-crystalline semiconductors.

DESCRIPTION OF THE SEVERAL DRAWINGS.

~~The invention will hereafter be described in greater detail with reference to embodiments. In the appended drawings:~~ The novel features which are considered to be characteristic of the invention are set forth with particularity in the appended claims. The invention itself, however, in respect of its structure, construction and lay-out as well as manufacturing techniques, together with other objects and advantages thereof, will be best understood from the following description of preferred embodiments when read in connection with the appended drawings, in which:

Fig. 1 depicts the first method step of fabricating a field effect transistor in accordance with the invention - growing of the free-standing semiconductor columns on a metallic conductive substrate;

Fig. 2 depicts the second method step - depositing a first insulating layer;

Fig. 3 depicts the third and fourth method step - depositing a first meal layer and a second insulating layer;

Fig. 4 depicts the fifth method step - planar etching;

Fig. 5 depicts the sixth method step - insulating the ends of the upwardly penetrating metal layer;

Fig. 6 depicts the seventh method step - depositing a second metal layer, a

cross-section of the completed structure of the transistor; and

Fig. 7 depicts a cross-section of an array of transistors which can be fabricated in accordance with the method.

DESCRIPTION OF THE PREFERRED EMBODIMENTS.

As shown in Fig. 1, vertically free-standing semiconductor columns 2 are initially grown on a conductive substrate 1 which may be flexible or rigid. This may be carried out by an unordered process as known, for instance, from /1/ in respect of the electro-chemical growth of ZnO-columns. Alternatively, ZnO could be deposited by vaporizing Zn or ZnO, see /2/. However, it is also possible so to prepare that in an ordered or unordered fashion nuclei are generated from which the columnar growth proceeds. Ni-dots, for instance, may be used for growing ZnO-columns /2/ or Ni-dots may be used for the vertical growth of C60-nano-tubes, see /3/, Fig. D. Ordered nuclei may be generated by lithographic methods, see /3/ or by non-lithographic methods, such as, for instance, dislocation stages of misaligned crystal surfaces. In the case of non-lithographically fabricated nuclei the size limitations inherent in lithography do not apply. The columnar growth is solely determined by the size of the nucleus. Semiconductor columns may, however, also be produced in etches ion trace channels of polymer films. Free-standing semiconductor columns are also formed after subsequent removal of the foil material, see /4/.

The semiconductor columns (nano-fibers / nano-tubes) grown on the substrates have hitherto gained importance chiefly for the construction of structural components for electron field emission, luminescence diodes and solar cells with an extremely thin absorption layer.

Aside from the materials mentioned for the semiconductor columns, such materials as GaP, see /5/, InAs, CdTe and others may also be used.

As shown in Fig. 2, an insulating layer 3 is deposited after the semiconductor columns 2 have been grown. The deposition may be carried out by spin-coating of a polymer or by vaporization, DVD (chemical vapor deposition) or other known processes of forming an insulating layer, such as, for instance, an oxide or nitride.

The insulating layer 3 also covers the side surfaces of the semiconductor columns 1. A first conductive metal layer 4, which later on constitutes the gate electrode of the transistor, is deposited on the insulating layer 3 by sputtering, vaporization, chemical vapor deposition or a similar process. Thereafter, a further insulating layer 5 is deposited (Fig. 3), and the upper layer of the laminate formed in this manner is etched planar (Fig. 4). This may be done by a horizontal ion beam (ion beam etching) or by plasma, chemical or electro-chemical etching processes of the kind sufficiently known in semiconductor technology. Thereafter, the upwardly penetrating ends of the metal layer 4 are insulated (Fig. 5). This may be carried out by etching back the metal protruding to the surface by a metal-specific etching step and by applying a further insulating layer which is planarized in turn. Alternatively, as shown in Fig. 5, the metal protruding to the surface may be converted to an insulator 6 by chemical oxidizing or nitriding. Finally, a second metal layer 7 is deposited (Fig. 6). This metal layer is electrically connected to the semiconductor column, and later on it serves as source electrode and drain electrode.

In the area of the center contact which acts as a gate electrode, a channel 8 is formed at the outside of the semiconductor column 2 which, provided the semiconductor column 2 is sufficiently thin, may extend over the entire thickness of the column.

Fig. 7 depicts an array of transistors. The gate electrode always surrounds the semiconductor column 2 in an annular fashion and is, overall, continuous. All electrodes (source, drain, gate) may be controlled as an array

or they may be divided by lithographic processes. Such arrays may be used in control circuits and displays. In an array, several hundreds of transistors are combined as an optical pixel.

The method allows fabrication of transistors with semiconductor columns in the range of 10 to 500 nm diameter. The heights of the semiconductor columns lie in the same range. At very small diameters, the transistor may be operated in a quantum regime.

List of Literature Cited

/1/ Koenenkamp et al.: Thin Film Deposition on Free-standing ZnO Columns; Appl. Phys. Lett. 77, No. 16 (16 October 2000), pp. 2275-2277.

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/3/ Teo et al.: Nanotech Conference, Santiago de Compostela, September 9-13, 2002-10-09.

/4/ Engelhardt, Koenenkamp: Electrodeposition of Compound Semiconductors in Polymer Channels of 100 nm Diameter; J. Appl. Phys., 90, No. 8 (15 October 2002), pp. 4287-4289.

/5/ Gudiksen/Lieber: Diameter-Selective Semiconductor Nanowires, J. Am. Chem. Soc. 122 (2000), pp. 8801-8802.

List of Reference Characters Used

1	Substrate
2	Semiconductor Column
3	Insulating Layer
4	Metal Layer
5	Insulating Layer
6	Insulator
7	Metal Layer
8	Channel

~~Patent Claims~~ What is claimed is:

1. A field effect transistor in which at least one vertically aligned semiconductor column (2) of a diameter in the nanometer range is present between a source electrode and a drain electrode (1, 7) and is annularly surrounded by a gate electrode with an insulating space between them,
characterized by the fact that
the semiconductor columns (2) are embedded in a first and a second insulating layer (3, 5) between which there is provided a metal layer (4) extending to the outside as a gate electrode whose ends penetrating through the second insulating layer (5) are partially converted to an insulator (6) or partially removed and filled by an insulating material.

2. A method of fabricating a field effect transistor in which at least one vertically aligned semiconductor column (2) of a diameter in the nanometer range is present between a source electrode and a drain electrode (1, 7) and is annularly surrounded by a gate electrode with an insulating space between them,
characterized by the fact that
- free-standing semiconductor columns are grown vertically on a conductive substrate;
- a first insulating layer is deposited on the semiconductor columns;
- a first conductive metal layer and a second insulating layer are deposited thereon;
- the developing laminates is etched planar to the point of the portion of the first metal layer covering the semiconductor columns is removed again;
- the end of the metal layer penetrating to the surface of the laminate are etched back in a metal-specific manner and a third insulating layer is deposited on the laminate with subsequent

renewed planar etching;

or

the ends of the metal layer penetrating to the surface of the laminate are converted to an insulator by oxidizing or nitriding; and

- finally depositing a second metal layer on the laminate.

3. The method of claim 2,
characterized by the fact that
the laminate or individual layers are divided into individual arrays by a lithographic process.

4. (Currently Amended) The method of claim 2 ~~or 3~~,
characterized by the fact that
the growing of the semiconductor columns is carried out electro-chemically.

5. (Currently Amended) The method of claim 2 ~~or 3~~,
characterized by the fact that
the growing of the semiconductor columns is carried out by sputtering.

6. (Currently Amended) The method of claim 2 ~~or 3~~,
characterized by the fact that
the growing of the semiconductor columns is carried out by a CVD process.

7. (Currently Amended) The method of claim 2 ~~or 3~~,
characterized by the fact that
the growing of the semiconductor columns is carried out by vaporization.

8. (Currently Amended) The method of claim 2 ~~or 3~~,
characterized by the fact that
the growing of the semiconductor columns is carried out in ion trace channels of a polymeric film which is subsequently removed.

~~Abstract~~ ABSTRACT OF THE DISCLOSURE

A field effect transistor ~~is known~~ in which at least one vertically arranged semiconductor column, with a diameter in the nanometer range, is located between a source and a contact and has an annular surround of a gate contact with retention of an insulation gap. A simplified production method is disclosed and the transistor produced thus is embodied such that the semiconductor columns ~~(2)~~ are embedded in a first and a second insulation layer ~~(3, 5)~~, between which a metal layer ~~(4)~~, running to the outside as a gate contact, is arranged, the ends of which, extending upwards through the second insulation layer ~~(5)~~, are partly converted into an insulator ~~(6)~~, or removed and replaced by an insulation material.